Agenda

Day 1
08.30: **Sign in**

09.00-10.30: Recommended reading, Impact of frequency & what drives it, Frequency- Analog *vs* Digital, Essentials of grounding, Noise- what is it, why it occurs, where energy travels in circuits, Impact of proper Grounding on Noise and EMI, Transmission lines and return current paths.

10.30-10.45: **Tea break**

10.45-12.15: Proper PCB plane assignment, Common misuse of planes, Noise & signal attenuation, Routing and reflections, Propagation time and velocity, Lumped *vs* distributed length lines, Transmission line impedance, No Cost impedance control, Impact of Nearby traces on impedance.

12.15-13.15: **Lunch break**

13.15-14.45: Reflection mode switching, Routing & termination styles, new thoughts on Line Termination, Best line routing styles, Impact of Long Ts in routed lines, Proper DDR routing, Vcc and Ground bounce, Signal attenuation factors, Impact of trace corners and vias.

14.45-15.00: **Tea break**

15.00-17.00: What is Cross Talk, Backward & forward cross talk, Realistic cross talk levels, Guard traces- Good or bad? Differential Pair basics, Differential Impedance, Diff pair crosstalk, Tight *vs* Loose coupling of lines, Length Matching of Differential pairs, Differential pair line termination.

19.00: Networking dinner

Day 2
09.00-10.30: Basic types of EMI, Antenna basics & PCB radiators, Control of Common Mode energy, Energy feeding plane edges, Basic component placement issues, Routing to control EMI & Noise, Impact of routing layer changes, Mixed analog & digital PCBs, Islands in Power planes, Impact of connector pin assignment.

10.30-10.45: **Tea break**

10.45-12.15: Power distribution Goals, Importance of Low PDN impedance, Inductance of Via and Planes, Impact of capacitor location, Decoupling PCBs with routed power, decoupling 4 Layer PCBs, Decoupling High layer count PCBs, Impact of IC design on delivery of power, Analog decoupling, Ferrites in power bus.

12.15-13.15: **Lunch break**

13.15-14.45: PC Board Stack-up basics, Boards to avoid at all costs, very good 4- & 6-layer boards, Excellent High layer count boards, I/O filtering, Setup and routing of I/O, Metal *vs* plastic enclosures, Slots in metal enclosures, Shielding of cables, Impact of I/O connector location, how many cables in the enclosure.

14.45-15.00: **Tea break**

15.00-17.00: Multiple PCBs in the system, Issues when using Chassis as a Heatsink, Proper Switch Mode power supply layout, Layout of SMPS to control EMI, Critical circuit loops including Feedback, Proper Grounding of Switch Node, Secondary methods to control EMI, Inductor types and proper mounting.

17.00: **Evaluation and certificate.**

Instructor: Richard Hartley

Rick Hartley, retired from L-3 Avionics, is the principal of RHartley Enterprises, through which he consults and teaches internationally. Rick's focus is on correct design of circuits and PC boards to prevent and/or resolve EMI, noise, and signal integrity problems. He has consulted with major corporations in the US and 14 other countries.

His career has focused on telecommunications, computers, and aircraft avionics, as well as medical, appliance and automotive circuits. Rick has taught seminars at numerous conferences, including the IEEE EMC Symposium, PCB West, AltiumLive, Freescale Technology Forum, IPC Apex/Expo and others.

He is on the Board of Directors of the 'Printed Circuit Engineering Association', is a past member of the Editorial Review Board of *Printed Circuit Design* Magazine and has written numerous technical papers and articles on methods to control noise, EMI and signal integrity.

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Organizer

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